**Test Case 1**

Assuming L = 4

S = 16

C = 4 lines

So,

|  |  |  |
| --- | --- | --- |
| Tag= 28 bits | Index = 2 bits | Offset = 2 bits |
| 00 | 00 | 00 |
| 01 |
| 10 |
| 11 |
| 01 | Same like above |
| 10 | Same like above |
| 11 | Same like above |
| 01 | Same like above | |
| 10 |
| 11 |

Example addresses needed to be accessed:

0x00 00 00 or 0 in decimal

And

00 00 01 = 1 in decimal

And

010101 = 21

And

010101 = 21

Mapping:

Address in decimal **mod** number of lines

For address 0, 0 mod 4 = 0, go check this data structure represented by the tag and index after your change the decimal address to binary, if it contains this address (Mem[0]), then it’s a hit.

Same for rest

For address 1, 1 mod 4 = 1

For address 21, 21 mod 4 = 1

|  |  |  |  |
| --- | --- | --- | --- |
| Tag= 28 bits | Index = 2 bits | Offset = 2 bits | Hit/Miss |
| 00 | 00 | 00 | Miss |
| 01 | Hit |
| 10 |  |
| 11 |  |
| 10 |  |  |
| 11 |  |  |
| 10 |  |  |
| 01 | 00 |  |  |
| 01 | 00 |  |
| 01 | Miss then Hit |
| 10 |  |  |  |
| 11 |  |  |  |

Now Assume you look for any miss in // this part has not been implemented

L-2 cache where,

L = 8,

S= 32

C = 4

So, now offset bits = 3

Index bits = 2

Tag bits = 27

So, in case of miss in L-1, you search in L-2 for

0 mod 4 = block 0 in L-2 cache

And when you miss the 21

You search again for 21 mod 4 = block 1 in L-2 cache.

What’s that going to affect?

The hit and miss ratio and the AMAT we keda